IN THE CLAIMS

Cancel claim 1 without prejudice or disclaimer, and add new claims 8-19 as follows:

1-7. (Canceled).

8. (New) A semiconductor device having a MISFET in a first region of a semiconductor substrate and a gate wiring in a second region of the semiconductor substrate, comprising:

the semiconductor substrate of n type conductivity;

a first semiconductor layer of n type conductivity serving as a drain of the MISFET, formed over the semiconductor substrate;

a second semiconductor layer of p type conductivity serving as a channel forming region of the MISFET, formed over the first semiconductor layer;

a third semiconductor layer of n type conductivity serving as a source of the MISFET, formed over the second semiconductor layer;

a first trench reaching from a top surface of the third semiconductor layer to the first semiconductor layer in the first region;

a gate insulating film of the MISFET formed inside the first trench;

a gate electrode of the MISFET formed on the fate insulating film;

a second trench formed in the second region;

a gate wiring formed in the second trench and outside the second trench in the second region;

wherein the gate electrode and gate wiring are electrically connected;

an upper portion of the gate insulating film is located over the top surface of the third semiconductor layer;

an upper portion of the gate electrode is located on the upper portion of the gate insulating film;

an insulating film is formed in the second region; and

the gate wiring outside the second trench is formed on the insulating film.

9. (New) The semiconductor device according to claim 8, further comprising:

an interlayer insulating film formed over the gate electrode and gate wiring;

a first conductive film and a second conductive film formed over the interlayer insulating film;

wherein the first conductive film is electrically connected to the second and third semiconductor layers; and

the second conductive film is electrically connected to the gate wiring.

10. (New) The semiconductor device according to claim 9, wherein the insulating film is not formed in the first region.

11. (New) The semiconductor device according to claim 9, wherein the insulating film is formed by a thermal oxidation method; and

the interlayer insulating film is formed by a deposition method.

12. (New) The semiconductor device according to claim 9, wherein the gate electrode and the gate wiring are comprised of a same layer.

13. (New) The semiconductor device according to claim 9, wherein a drain electrode is formed on a back surface of the semiconductor substrate.

14. (New) The semiconductor device according to claim 9, wherein a field insulating film is formed in the second region; and

a portion of the gate wiring is located on the field insulating film.

15. (New) The semiconductor device according to claim 9, wherein an epitaxial layer is formed over the semiconductor substrate;

the first, second and third semiconductor layers are formed in the epitaxial layer.

16. (New) The semiconductor device according to claim 15, wherein the upper portion of the gate insulating film is located on the top surface of the epitaxial layer; and

the top portion of the gate electrode is located on the top portion of the gate insulating film.

17. (New) The semiconductor device according to claim 16, wherein the insulating film is formed on the top surface of the epitaxial layer in the second region.

18. (New) A semiconductor device having a MISFET in a first region of a semiconductor substrate and a gate wiring in a second region of the semiconductor substrate, comprising:

the semiconductor substrate of a first type conductivity;

a first semiconductor layer of the first type conductivity formed over the semiconductor substrate;

a second semiconductor layer of a second type conductivity, which is opposite to the first type conductivity, formed over the first semiconductor layer;

a third semiconductor layer of the first type conductivity, formed over the second semiconductor layer;

a first trench reaching from a top surface of the third semiconductor layer to the first semiconductor layer in the first region;

a gate insulating film of the MISFET formed inside the first trench;

a gate electrode of the MISFET formed on the gate insulating film;

a second trench formed in the second region;

a gate wiring formed in the second trench and outside the second trench in the second region;

wherein the gate electrode and gate wiring are electrically connected;

an upper portion of the gate insulating film is located over the top surface of the third semiconductor layer;

an upper portion of the gate electrode is located on the upper portion of the gate insulating film;

an insulating film is formed in the second region; and

the gate wiring outside the second trench is formed on the insulating film.

19. (New) The semiconductor device according to claim 18, further comprising:

an interlayer insulating film formed over the gate electrode and gate wiring;

a first conductive film and a second conductive film formed over the interlayer insulating film;

wherein the first conductive film is electrically connected to the second and third semiconductor layers; and

the second conductive film is electrically connected to the gate wiring.